



Docket No.: 50090-265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED PATENT  
OCT 08 2002 #1 A  
TECHNOLOGY CENTER 2800  
PERMAN'S

In re Application of

Kiyotoshi UEDA, et al.

Serial No.: 09/766,845

Filed: January 23, 2001

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR  
INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT  
MANUFACTURED THEREBY

Group Art Unit: 2829

Examiner: P. Patel

AMENDMENT

Commissioner for Patents  
Washington, DC 20231

Sir:

In response to the Office Action dated July 17, 2002, reconsideration is respectfully requested in light of the following remarks.

IN THE CLAIMS:

Claim 7 now reads as follows:

7. (Amended) A semiconductor integrated circuit testing apparatus for testing signal wiring lengths connecting to all pins of a semiconductor integrated circuit, comprising:  
a signal generator configured to generate a measuring signal and to transmit the measuring signal to all pins of the semiconductor integrated circuit; and  
correcting means for correcting input waveform timing based on measurements of the measuring signal.

of what